REMARKS

Claims 1-26 and 29-40 are all the claims pending in the application. In this Amendment Applicant amendments claims 1, 17, 33, 34 and 37-40. No new matter is added. Claims 8-15 and 22-26 are withdrawn from consideration.

Claim rejection under 35 U.S.C. § 112, second paragraph

Claims 37-40 are rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Applicant traverses the rejection as follows.

In view of the amendment to claims 37-40 submitted herewith, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. § 112, second paragraph rejection.

Claim rejection under 35 U.S.C. § 103(a)

Claims 1, 3-4, 17-19, 21, 29-35 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yanagi et al. (U. S. Patent No. 7,002,541 B2; hereinafter "Yanagi") in view of Okajima (U.S. Patent No. 5,793,680; hereinafter "Okajima") and Yatabe et al. (Japanese Publication No. 2001-051662 as translated by U.S. Patent No. 6,633,287 B1; hereinafter "Yatabe").

Claims 5, 20 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yanagi in view of Okajima, Yatabe and Park et al. (U.S. Patent No. 7,133,034; hereinafter "Park").

Claims 2, 6-7, 16, 36 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yanagi in view of Okajima, Yatabe, Kubota et al. (U.S. Publication No.

2002/0075249; hereinafter "Kubota") and Nagai (U.S. Patent No. 6,011,355; hereinafter "Nagai"). and Park.

Applicant traverses the rejection as follows.

Claim 1

In the Amendment filed September 15, 2010, Applicant argued that Yatabe does not teach or suggest the feature of "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply," as recited in claim 1.

In response, the Examiner asserts that Yatabe allegedly teaches the concept of having a high level (FIG. 5, item VSP) of a signal passing through a signal line that is higher than the high level voltage signal supplied by the first voltage (FIG. 5, item Vcc) and a low level of a signal passing through a signal line (Fig. 5, item VSN) that is lower than the low level voltage signal supplied by the second voltage supply (FIG. 5, item GND). See page 3, lines 1-4 of the Office Action. Applicant respectfully disagrees with the Examiner for at least the following reasons.

According to claim 1, "signal" is described as the signal which passes through "the at least one signal line," which is connected to the gate terminals of the first and the second transistors. Further, the high level voltage of the signal is higher than the high level voltage supplied from the first power supply and the low level voltage of the signal is lower than the low level voltage supplied from the second power supply. These claimed features of claim 1, are described in an exemplary non-limiting embodiment in FIG. 5 of the present application. FIG. 5

and the corresponding description in the specification describes that the low level of COMD < VCOML < VCOMH < high level of COMD and the COMD is the signal which passes through the one signal line.

On the other hand, although FIG. 5 of Yatabe discloses a relationship between the high level voltage and the low level voltage, it does not teach or suggest "a high level of a signal passing through the at least one signal line is higher than the high level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply." In particular, even if, *assuming arguendo*, FIG. 5 of Yatabe discloses VSN < GND < Vcc <VSP, Yatabe does not teach or suggest that a high level voltage of a signal line is VSP and a low level voltage of the signal line is VSN. That is, Yatabe does not teach or suggest a signal line, which has VSP as high level voltage and VSN as low level voltage.

For instance, FIG. 11 of Yatabe, which shows circuit diagram of the inverter circuit used in the supply circuit does not teach or suggest that the voltage level of the signals of /A and B are VSP and VSN. Applicant respectfully submits that even if, *assuming arguendo.* the "one capacitance load" of claim 1 corresponds to "Cp" shown in FIG. 11 of Yatabe, "the first and the second transistor" of claim 1 corresponds to "Tp1" and "Tp2" of Yatabe, and "the first and the second power supply" correspond to "VSP" and "Vcc" respectively, Yatabe does not teach or suggest that the high level of the gate signals /A and B of Tp1 and Tn1 are higher than VSP and the low level of these signals are lower than Vcc. Since there is no description regarding the high voltage which is higher than VSP in Yatabe, Yatabe does not teach or suggest the features of "a high level of a signal passing through the at least one signal line is higher than the high

level voltage signal supplied by said first voltage supply and a low level of the signal passing through the signal line is lower than the low level voltage signal supplied by said second voltage supply,"

Moreover, even if, *assuming arguendo*, "the first and the second transistors" of claim 1 correspond to "Tp2" and "Tn2" respectively, and "the first and the second power supplies" of claim 1 correspond to "GND" and "VSN" of Yatabe, respectively, since there is no description regarding the voltage which is lower than VSN in Yatabe , the low voltage of the gate signals /A and B of Tp2 and Tn2 could not be raised higher than VSN.

In addition, Applicant respectfully disagrees with the Examiner's assertion that the description of the connection of the signal line with the first power supply and the second power supply is unclear. For instance, claim 1 clearly describes that the first power supply is connected to a drain or a source terminal of the first transistor, the second power supply is connected to a drain or a source terminal of the second transistor, and the signal line is connected to each gate of the first and the second transistor. As such, the claimed features of the signal line are clearly recited in claim 1.

In view of the above Applicant respectfully submits that claim 1 is patentable over the cited combination of references.

Claims 17, 33 and 34

Applicants respectfully submit that claims 17, 33 and 34 recite subject matter analogous to claim 1, and therefore are allowable for at least analogous reasons claim 1 is allowable.

Claims 3-4, 18-19, 21, 29-32, 35 and 37-40

Applicants submit that claims 3-4, 18-19, 21, 29-32, 35 and 37-40 depend from one of the independent claims that have been shown to be allowable, and therefore these claims are allowable at least by virtue of there dependency and the additional features recited therein.

With regard to claims 29-32, Applicant respectfully submits that the features of these claims are not disclosed in the combination of Yanagi, Okajima and Yatabe.

For instance, resistances 5a and 5b in an offset voltage setting section 5 shown in FIG. 1 of Yanagi are used for dividing the voltage of Vrefl. However, this does not teach or suggest a level shift circuit. Further, element 60 of FIG. 14 of Okajima corresponds to a CLOCK-PULSE-ARRANGEMENT DETERMINATION UNIT. However, there is no description for item 60 to have the function of conversion of the level of the input signal, and therefore does not teach or suggest a level shift circuit as recited in claims 29-32.

Claims 5 and 20

Applicant submits that since claims 5 and 20 depend from one of the claims that have been shown to be allowable and since Park does not teach or suggest the features of claim 1 missing in Yanagi, Yatabe and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

With regard to claims 5 and 20, the Examiner cites Park for allegedly disclosing "wherein a high-level voltage of each signal of said signal line and said inversion signal line is a high-level line voltage of said gate driver and wherein a low-level voltage of each signal of said signal line

and said inversion signal line is a low-level line voltage of said gate driver." Applicant respectfully disagrees with the Examiner for at least the following reasons.

Applicant respectfully submits that although Park discloses a signal controller input to the driver (FIG. 1), Park does not teach or suggest a high-level voltage of each signal of said signal line and said inversion signal line is a high-level line voltage of said gate driver and wherein a low-level voltage of each signal of said signal line and said inversion signal line is a low-level line voltage of said gate driver, as recited in claims 5 and 20.

Claims 2, 6-7, 16, 36

Applicants submit that since claims 2, 6-7, 16, 36 depend from one of the claims that have been shown to be allowable and since Kubota, Nagai and Park do not teach or suggest the features of claim 1 missing in Yanagi, Yatabe and Okajima, these claims are also allowable at least by virtue of their dependency and the additional features recited therein.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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